* D-Latch
  + Level-triggered - stores whatever is on input when write-enable goes from true to false
* Master-Slave
  + 2 D latches in series, ensures that only one write occurs per clock cycle
* Register - can store multiple bits
* Finite State Machines
  + Implementation
  + Types:
    - Binary Encoded: encode state as binary number and use decoder to generate a line for each state
      * Slower, more complicated
    - One Hot